ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 7, July 2015

Low Power Full Adder Circuit Implementation using Transmission Gate

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Abstract: In this paper, the power consumption of a conventional full adder circuit is reduced by using transmission gate at the place of pass transistor logic (NMOS or PMOS). This circuit is designed using 100nm technology parameters.

Keywords: power; full adder circuit; transmission gate; pass transistor; NMOS; PMOS.

I. INTRODUCTION

The main objective of this paper is to reduce the power consumption, which is showing an increasing growth with the scaling down of the technologies. In conventional full adder circuits, we use CMOS technology i.e. PMOS and NMOS are used as a switch in complementary mode. Such applications of NMOS and PMOS as a switch is called pass transistor logic. In Transmission Gates, both NMOS and PMOS transistors are combined in parallel fashion. When performance of both the circuits was compared, transmission gate circuit consumed less power as compared to the pass transistor circuit designed using CMOS logic.

This paper is organized under the headings, pass transistor logic, Transmission Gates, Conventional Full Adder circuit using CMOS technology, Low power full adder circuit using Transmission Gate, Results, Conclusion and References.

II. PASS TRANSISTOR LOGIC

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic.

In conventional logic families input is applied to gate terminal of transistor but in PTL it is also applied to source/drain terminal. When used as pass transistor, the device may conduct current in either direction.

A. Basic Principle of Pass Transistor Circuit

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal Vin. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion load NMOS inverter obviously assumes a logic-low or a logic-high level, depending upon the voltage V_x.

NMOS Pass Transistor- Logic '1' transfer:

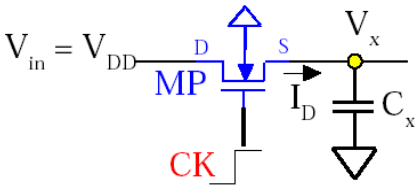

Figure 1

NMOS Pass Transistor- Logic '0' transfer:

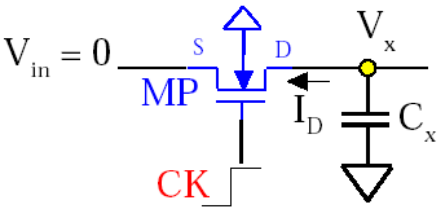

Figure 2

Therefore, **NMOS passes- a strong '0' and weak '1'**. Similarly, it can be shown for **PMOS** that it **passes- a strong '1' and weak '0'**.

B. Properties of Pass Transistor

- Very efficient in use of transistors.
- Potentially very efficient layouts result.
- Pass transistors can usually be minimum size devices.
- Propagation delays can become large in long series string
- Static power dissipation is unaffected
- Dynamic power dissipation may be decreased.

III. TRANSMISSION GATES

A transmission gate is defined as an electronic element that will selectively block or pass a signal level from the input to the output. This solid-state switch is comprised of a PMOS transistor and NMOS transistor.

The transmission gate consists of two MOSFETs, one n-channel responsible for correct transmission of logic zeros, and one p-channel, responsible for correct transmission of logic ones.

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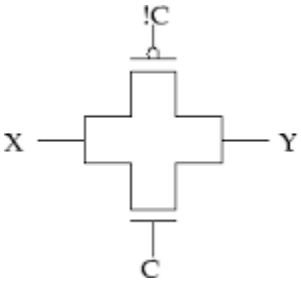

Figure 3: Transmission Gate Circuit

When C = 1, X and Y are connected, both logic zero and logic one are passed without degradation.

A transmission gate has three inputs, called source, n-gate, and p-gate; and it has one output, called drain. The two transistors, an NMOS and a PMOS are connected in parallel configuration.

When the control input is a logic zero (negative power supply potential), the gate of the NMOS is also at a negative supply voltage potential. The gate terminal of the PMOS is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (X or Y) a voltage is applied, the gate-source voltage of the NMOS is always negative, and the PMOS is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off. When the control input is a logic one, so the gate terminal of the NMOS is located at a positive supply voltage potential. By the inverter, the gate terminal of the PMOS is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts.

One of the switching terminals of the transmission gate is raised to a voltage near the negative supply voltage, a positive gate-source voltage (gate-to-drain voltage) will occur at the NMOS, and the transistor begins to conduct, and the transmission gate conducts. The voltage at one of the switching terminals of the transmission gate is now raised continuously up to the positive supply voltage potential, so the gate-source voltage is reduced (gate-drain voltage) on the NMOS, and this begins to turn off. At the same time, the PMOS has a negative gate-source voltage (gate-to-drain voltage) builds up, whereby this transistor starts to conduct and the transmission gate switches.

Thereby it is achieved that the transmission gate passes over the entire voltage range. Transmission gates are used in order to realize electronic switches and analog multiplexers.

IV. ADDER IMPLEMENTATION

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (X, Y and Z) and two 1-bit outputs -Sum (S)and Carry(C).

The relations between the inputs and the outputs are expressed as:

$$S = XY'Z' + X'YZ' + XYZ + X'Y'Z$$

$$C = XY + YZ + XZ$$

IV.(A) CONVENTIONAL FULL ADDER CIRCUIT USING CMOS TECHNOLOGY

Conventional CMOS Circuit consists of two functional blocks - pull-up and pull-down. Pull-up functional block is implemented with PMOS transistors and pull down functional block is implemented with NMOS transistors. Following is the circuit:

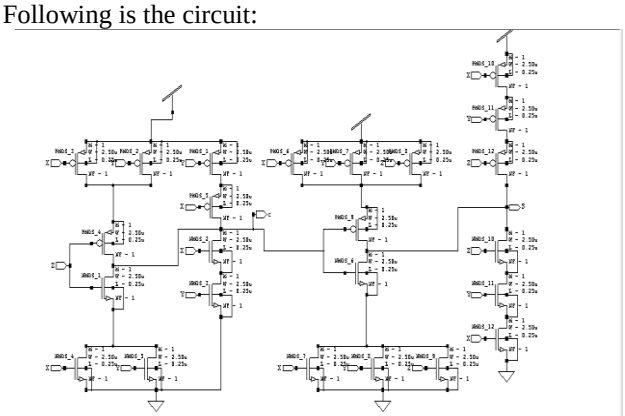

Figure 4: Conventional CMOS Full Adder

IV(B) LOW POWER FULL ADDER CIRCUIT USING TRANSMISSION GATE

Transmission gates are widely used as CMOS design style to implement digital function.

Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses both NMOS and PMOS transistors connected in parallel where as pass transistor logic uses only one type of transistor i.e. either NMOS or PMOS. Following is the circuit:

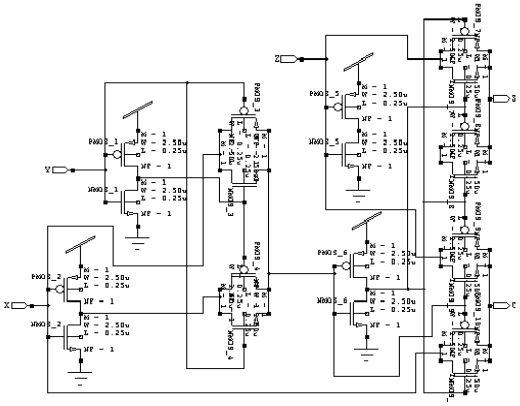

Figure 5: Full Adder Using Transmission Gate

V. RESULTS

In order to estimate the power dissipation of the different circuits present in previous section, we implement all the circuits by using Tanner tools(S-edit, T-SPICE) using 100nm technology parameters. The simulation waveforms for both the circuits are shown.

The average power consumed by both the circuits is calculated and value of peak voltage that is V_{dd} is 1.2V.

- **Power dissipation of Conventional CMOS adder is: 1.187164e-003 watts**
- **Power dissipation of Full adder using Transmission Gate is: 3.824165e-005 watts**

DOI 10.17148/IJARCCE.2015.4741

ISSN (Online) 2278-1021
ISSN (Print) 2319-5940

International Journal of Advanced Research in Computer and Communication Engineering
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This confirms that the circuit of full adder designed using Transmission Gate consumes less power as compared to the circuit of conventional full adder using Pass Transistor Logic i.e. using CMOS design.

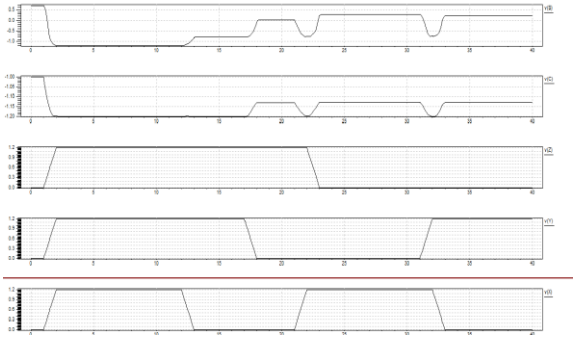

Figure 6: Simulated Waveform of Conventional CMOS Adder

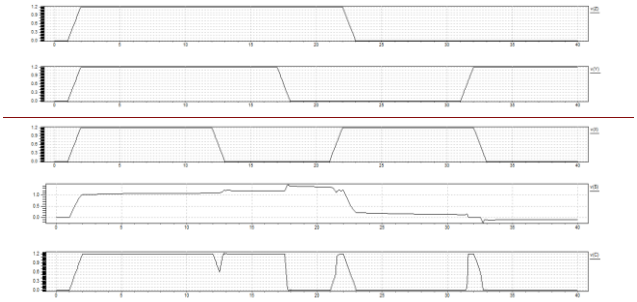

Figure 7: Simulated Waveform of Full Adder using Transmission Gate

VI. CONCLUSION

Two different types of full adders are presented. In this paper we compared the performance of transmission gate full adder and full adder circuits with traditional CMOS circuits (having pass transistor logic). The simulation results show that designs based on transmission gate gives superior performance when compared to performance in terms of power. That is why transmission gate circuits have wide range of applications.

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